Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BALANCE**
2. **INPUT –**
3. **INPUT +**
4. **V –**
5. **OUTPUT**
6. **V +**
7. **NC**
8. **BALANCE**

**.093”**

**.057”**

**1**

**2**

**3**

**4**

**8**

**7**

**6**

**5**

**1415X**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 1415X**

**APPROVED BY: DK DIE SIZE .057” X .093” DATE: 10/6/22**

**MFG: ANALOG DEVICES THICKNESS .015” P/N: OP77NBC**

**DG 10.1.2**

#### Rev B, 7/19/02